AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A thin film transistor substrate in a liquid crystal display provided with a data line for applying a data signal, a gate line for applying a gate signal, and a pixel electrode for driving a liquid crystal cell, said substrate comprising:

a gate dummy pattern formed so as to extend vertically from the gate line and to overlap with the data line and the pixel electrode, the gate dummy pattern being integrated with the [[data]] **gate** line.

2. (Previously Presented) The thin film transistor substrate according to claim **1**, wherein the gate dummy pattern is formed in such a manner to overlap with one side of the data line and the edge of the pixel electrode adjacent thereto.

3. (Original) The thin film transistor substrate according to claim **2**, wherein the gate dummy pattern is used as a redundancy electrode for electrically connecting the gate line to the broken data line.

4. (Currently Amended) The thin film transistor substrate according to claim **3**, wherein the gate dummy pattern includes a recess ~~connected to the gate line and~~ formed to permit a repair **by disconnection of the gate dummy pattern from the gate line**.

5. (Original) The thin film transistor substrate according to claim **1**,

wherein the gate dummy pattern is used as a black matrix.

6. (Original) The thin film transistor substrate according to claim **1**, further comprising:

a storage capacitor defined by a horizontal overlapping part between the gate line and the pixel electrode.

7. (Currently Amended) The thin film transistor substrate according to claim **4**, further comprising:

a protrusion **protruded from the data line** formed in such a manner **as** to overlap with the [[hole]] **recess**, thereby shutting off a light leaked between the gate dummy pattern and the gate line.

8. (Currently Amended) The thin film transistor substrate according to claim **1**, wherein the gate dummy pattern is formed on the lower substrate **at each side of the data line,** ~~having~~ **wherein** a gate-insulating layer ~~at each side of the data line~~ **is formed between the gate dummy pattern and the data line**.

9. (Currently Amended) The thin-film transistor substrate according to claim **4**, wherein the recess is provided at a cutting part for ~~breaking~~ **breaking** the ~~gate line and the~~ gate dummy pattern **from the gate line** in such a manner ~~as to~~ **that the recess is** not [[be]] overlapped with the data line.

10. (Currently Amended) A thin film transistor substrate in a liquid crystal display provided with a data line for applying a data ~~signals~~ **signal**, a gate

line for applying a gate signal, and a pixel electrode for driving a liquid crystal cell, said substrate comprising:

a gate dummy pattern formed so as to extend vertically from the gate line and to overlap by from about 0.5-1 μm with the data line and the pixel electrode, to thereby serve as a black matrix to shut off light leaked between said data line and said pixel electrode**, the gate dummy pattern being integrated with the gate line**.

11. (Previously Presented) The thin film transistor substrate according to claim **10**, wherein the gate dummy pattern is formed in such a manner to overlap with one side or both sides of the data line and the edge of the pixel electrode adjacent thereto.

12. (Previously Presented) The thin film transistor substrate according to claim **11**, wherein the gate dummy pattern is used as a redundancy electrode for electrically connecting the gate line to the broken data line.

13. (Currently Amended) The thin film transistor substrate according to claim **12**, wherein the gate dummy pattern includes a [[hole]] **recess** ~~connected to the gate line and~~ formed to permit a repair **by disconnection of the gate dummy pattern from the gate line**.

14. (Canceled)

15. (Previously Presented) The thin film transistor substrate according to claim **10**, further comprising:

a storage capacitor defined by a horizontal overlapping part between the gate line and the pixel electrode.

16. (Currently Amended) The thin film transistor substrate according to claim [[**14**]] **13**, further comprising:

a protrusion formed in such a manner to overlap with the [[hole]] **recess**, thereby shutting off a light leaked between the gate dummy pattern and the gate line.

17. (Currently Amended) The thin film transistor substrate according to claim **10**, wherein the gate dummy pattern is formed on the lower substrate **at each side of the data line,** having **wherein** a gate-insulating layer ~~at each side of the data line~~ **is formed between the gate dummy pattern and the data line**.

18. (Currently Amended) The thin-film transistor substrate according to claim **10**, wherein the recess is provided at a cutting part for breaking **breaking** the ~~gate line and the~~ gate dummy pattern **from the gate line** in such a manner ~~as to~~ **that the recess is** not [[be]] overlapped with the data line.

19. (New) The thin-film transistor substrate according to claim 1,

wherein the gate dummy pattern is formed in such a manner that an edge of the data line overlaps with one side of the gate dummy pattern and an edge of the pixel electrode overlaps with another side of the gate dummy pattern.

20. (New) The thin-film transistor according to claim 10,

wherein the gate dummy pattern is formed in such a manner that an edge of the data line overlaps with one side of the gate dummy pattern and an edge of the pixel electrode overlaps with another side of the gate dummy pattern.